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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	Art Unit: 2811
Kinzer, et al.	Examiner: Nadav, Ori
Serial No.: 10/613,326	
Filed: July 3, 2003	
For: **Vertical Conduction Flip-Chip Device with Bump contacts on Single Surface**	

RESPONSE TO NOTIFICATION OF NON-COMPLIANT APPEAL BRIEF

Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir/Madam:

In the "Notification of Non-Complaint Appeal Brief" mailed on July 29, 2009, in the above-identified patent application, the Examiner has stated that the Appeal Brief filed on April 27, 2009 (filed by a previous law firm) is defective for failure to comply with one or more of the provisions of 37 CFR 41.37. In response, Applicants hereby amend the Appeal Brief filed on April 27, 2009 to replace the previous "Summary of Claimed Subject Matter" with the attached amended "Summary of Claimed Subject

Matter," and respectfully submit that the Appeal Brief, as amended herein, is now compliant with 37 CFR 41.37, including 37 CFR 41.37(c)(1)(v).

Respectfully Submitted,
FARJAMI & FARJAMI LLP

Date: 8/14/09

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V. SUMMARY OF CLAIMED SUBJECT MATTER

A. Claim 1

Independent claim 1 defines a flip chip semiconductor device including a silicon wafer (e.g., silicon die 30 in Figures 1-4 and 6-8) having parallel first and second major surfaces (e.g., respective top and bottom surfaces of silicon die 30 in Figures 1, 4, and 6-8). *See*, e.g., page 5, lines 2-5, 16, and 19-20 and Figures 1-4 and 6-8 of the present application. The flip chip semiconductor device further includes at least one P region (e.g., P type junction receiving layer 51 in Figures 4 and 6-8) and at least one N region (e.g., N type base or channel diffusion 52 in Figure 4) which meet at a PN junction within the silicon wafer. *See*, e.g., page 5, lines 22-25 and Figures 4 and 6-8 of the present application.

The flip chip semiconductor device further includes first and second laterally spaced and metallized layers (e.g., source contact 31 and drain contact 32 in Figures 2-4) formed on the first major surface (e.g. the top surface of silicon die 30), where each of the first and second metallized layers is connected to one of the P region (e.g., P type junction receiving layer 51 in Figures 4 and 6-8) and the N region (e.g., N type base or channel diffusion 52 in Figure 4) and a bottom metallized layer extending across the second major surface (e.g., the bottom surface of silicon die 30). *See*, e.g., page 6, lines 8-15, page 8, lines 3-5, and Figures 2-4 and 6-8 of the present application. For example, source electrode 31 can be connected to N diffusion 52 through contact openings 81 and 82 and N^+ contact diffusions formed at the bottoms of contact openings 81 and 82 and drain

electrode 32 can be connected to P type junction receiving layer 51 through P^+ sinker diffusion 90 (shown in Figure 7) or through conductive polysilicon 92 (shown in Figure 8). *See*, e.g., page 6, lines 7-15 and Figures 4 and 7-8 of the present application.

As disclosed in the present application, Figure 4 shows a schematic representation in which drain electrode 32 is shown as contacting an upwardly extending portion of P^+ substrate 50. As further disclosed in the present application, in practice, the contact from drain electrode 32 to P^+ substrate 50 is made as shown in Figure 7 or Figure 8. *See*, e.g., page 7, lines 1-6 of the present application.

The flip chip semiconductor device further includes a third metallized layer (gate electrode metal pad 33 in Figure 2) atop the first major surface which is laterally spaced from the first and second metallized layers (e.g., source electrode 31 and drain electrode 32 in Figures 2-4), where the first, second, and third metallized layers comprise source, drain, and gate electrodes respectively of a MOSgated device, and where a current path inside the silicon wafer from the source electrode to the drain electrode includes a vertical component which is generally perpendicular to the first major surface. *See*, e.g., page 5, lines 12-15 and 21-22, page 6, lines 14-15, page 7, lines 7-14, and Figures 2-4 of the present application.

B. Claim 12

Independent claim 12 defines substantially similar subject matter (i.e., a flip chip semiconductor device) as independent claim 1, with a difference being that claim 12 specifies a plurality of contact bumps connected to each of the first and second metallized

layers (e.g., solder balls S situated on source electrode 101 and solder balls D situated on drain electrode 102 or solder balls D situated on drain electrode 103 in Figure 10), where the plurality of contact bumps connected to the first metallized layer (e.g., source electrode 101 in Figure 10) are aligned along a first straight row (e.g., a row of solder balls S situated on source electrode 101 in Figure 10), and where the plurality of contact bumps connected to the second metallized layer (e.g., drain electrode 103 in Figure 10) are aligned along a second straight row (e.g., the row of solder balls D situated on drain electrode 102 or the row of solder balls D situated on drain electrode 103 in Figure 10). *See*, e.g., page 8, lines 6-12 and Figure 10 of the present application.

C. Claim 16

Claim 16 depends from independent claim 12 and, therefore, includes the flip chip semiconductor device of independent claim 12 discussed above. In addition, claim 16 specifies that the first and second rows are parallel to one another (e.g., a row of vertically oriented solder balls S on source electrode 101 is in a parallel orientation with the row of solder balls D on either drain electrode 102 or drain electrode 103 in Figure 10). *See*, e.g., page 8, lines 10-15 and Figure 10 of the present application.

D. Claim 17

Claim 17 depends from independent claim 12 and, therefore, includes the flip chip semiconductor device of independent claim 12 discussed above. In addition, claim 17 specifies that the silicon wafer is a rectangular wafer (e.g., die 130 in Figure 14) having

an area defined by a given length and a given width, where the length is greater than the width, and where the first and second rows of bumps (e.g., a row of electrode bumps S1 on FET 140 and a row of electrode bumps S2 on FET 141 in Figure 14) are parallel to one another and symmetric about a diagonal line (e.g., dotted diagonal line 150 in Figure 14) across the wafer. *See*, e.g., page 9, line 13-27 and Figure 10 of the present application.

E. Claim 27

Independent claim 27 defines a semiconductor device including a silicon die (e.g., silicon die 30 in Figures 1-4 and 6-8) having first and second parallel surfaces (e.g., respective top and bottom surfaces of silicon die 30). *See*, e.g., page 5, lines 1-7, 16, and 19-20 and Figures 1-4 and 6-8 of the present application. The semiconductor device further includes a region (e.g., P type junction receiving layer 51 in Figures 4 and 6-8) of one conductivity type extending from the first surface and into the body of the die. *See*, e.g., page 5, lines 22-24 and Figures 4 and 6-8 of the present application. The semiconductor device further includes a junction pattern defined in the device formed by a plurality of laterally spaced diffusions (e.g., N type base or channel diffusion 52, which is divided into laterally spaced diffusions by trenches 60 and 61 in Figure 4) of the other conductivity type into the region of one conductivity type (e.g., P type junction receiving layer 51). *See*, e.g., page 5, lines 21-28 and Figure 4 of the present application.

The semiconductor device further includes a first conductive power electrode (e.g., source electrode 31 in Figures 1-4) formed atop the first surface (e.g., the top surface of

silicon die 30) and in contact with the plurality of laterally spaced diffusions (e.g., source electrode 31 is in electrical contact with the laterally spaced diffusions through openings 81 and 82 and N^+ regions in Figure 4). *See*, e.g., page 5, lines 12-14, page 6, lines 8-10, and Figures 1-4 of the present application. The semiconductor device further includes a second conductive power electrode (e.g., drain electrode 32 in Figures 2-4 and 7-8) formed atop the first surface which is laterally spaced apart from the first conductive electrode (e.g., source electrode 31) and in electrical contact with the body of the die through a high conductivity element (e.g., P^+ "sinker" diffusion 90 in Figure 7 or conductive polysilicon 92 in Figure 8). *See*, e.g., page 5, lines 12-15, page 7, lines 1-6, and Figures 2-4 and 7-8 of the present application.

As disclosed in the present application, Figure 4 shows a schematic representation in which drain electrode 32 is shown as contacting an upwardly extending portion of P^+ substrate 50. As further disclosed in the present application, in practice, the contact from drain electrode 32 to P^+ substrate 50 is made as shown in Figure 7 or Figure 8. *See*, e.g., page 7, lines 1-6 of the present application.

The semiconductor device further includes at least one solder ball connector formed atop each of the first and second conductive electrodes respectively (e.g., source contact ball 40 on source electrode 31 and drain contact balls 41 and 42 on drain electrode 32 in Figure 3). *See*, e.g., page 5, lines 17-19 and Figure 3 of the present application. The current path inside the silicon die (e.g., silicon die 30) from the first conductive electrode (e.g., source electrode 31) to the second conductive electrode (e.g., drain electrode 32) has a vertical component which is generally perpendicular to the first

surface (e.g., the top surface of silicon die 30). *See*, e.g., page 7, lines 7-14 of the present application.

F. Claim 28

Claim 28 depends from independent claim 27 and, therefore, includes the semiconductor device of independent claim 27 discussed above. In addition, claim 28 specifies that the high conductivity element is a sinker diffusion (e.g., P^+ "sinker" diffusion 90 in Figure 7) of higher conductivity than said body region (e.g., P type junction receiving layer 51 in Figures 4 and 6-8). *See*, e.g., page 7, lines 1-5 and Figures 4 and 6-7 of the present application.

G. Claim 29

Claim 29 depends from independent claim 27 and, therefore, includes the semiconductor device of independent claim 27 discussed above. In addition, claim 29 specifies that the high conductivity element is a metallic material (e.g., metal 92 in Figure 8) residing in a trench (e.g., trench 91 in Figure 8) formed in the body (e.g., P type junction receiving layer 51 in Figures 4 and 6-8) of the die (e.g., silicon die 30). *See*, e.g., page 7, lines 1-6 and Figures 4 and 6-8 of the present application.